CLAIMS:

1. A level shifting circuit comprising

a first MOS transistor whose first terminal is connected to a first port and whose second terminal is connected to a second port,

a second MOS transistor of the same conductivity type as the aforementioned first MOS transistor, whose first terminal is connected to a power supply voltage terminal that supplies a power supply voltage corresponding to a reference logic level and whose second terminal and gate terminal are both connected to the gate terminal of the aforementioned first MOS transistor, and

a bias means for supplying a prescribed bias voltage below the aforementioned power supply voltage to the gate terminal of the aforementioned first MOS transistor.

2. The level shifting circuit of Claim 1, comprising a first clamping circuit connected between the aforementioned power supply voltage terminal and the aforementioned first port in order to clamp the potential at the aforementioned first port close to the aforementioned reference logic level.

3. The level shifting circuit of Claim 1, comprising a first switch wherein the aforementioned first clamping circuit is turned off when the potential levels of the aforementioned first and second ports have logic levels different from the aforementioned reference logic level, and it is turned on when the potential of the aforementioned first and/or the second port has a logic level equal to the aforementioned reference logic level.

4. The level shifting circuit of Claim 2 or 3, wherein the aforementioned first clamping circuit is provided with a first diode for allowing a current to flow in the forward direction from the aforementioned power supply voltage terminal to the aforementioned first port.

5. The level shifting circuit of one of Claims 2-4, wherein the aforementioned first clamping circuit is provided with a first constant current source circuit for allowing a constant

current to flow from the aforementioned power supply voltage terminal to the aforementioned first port.

6. The level shifting circuit of one of Claims 1-5 comprising a second clamping circuit connected between the aforementioned power supply voltage terminal and the aforementioned second port in order to clamp the potential of the aforementioned second port near the aforementioned reference logic level.

7. The level shifting circuit of Claim 6, comprising a second switch wherein the aforementioned second clamping circuit is turned off when the potential levels of the aforementioned first and the second ports have logic levels different from the aforementioned reference logic level, and it is turned on when the potential of the aforementioned first and/or the second port is logically equal to the aforementioned reference logic level.

8. The level shifting circuit of Claim 6 or 7, wherein the aforementioned second clamping circuit is provided with a second diode for allowing a current to flow in the forward direction from the aforementioned power supply voltage terminal to the aforementioned second port.

9. The level shifting circuit of described under one of Claims 6-8, wherein the aforementioned second clamping circuit is provided with a second constant current source circuit for allowing a constant current to flow from the aforementioned power supply voltage terminal to the aforementioned second port.

10. The level shifting circuit of one of Claims 1-9, comprising a third diode whose anode is connected to the aforementioned first port, and whose cathode is connected to the gate terminal of the aforementioned first MOS transistor.

11. The level shifting circuit of Claim 10, comprising a first resistor connected in series with the aforementioned third diode between the aforementioned first port and the gate terminal of the aforementioned first MOS transistor.

12. The level shifting circuit of Claim 10, comprising a third constant current source circuit connected in series with the aforementioned third diode between the aforementioned first port and the gate terminal of the aforementioned first MOS transistor.

13. The level shifting circuit of one of Claims 1-12, comprising a fourth diode whose anode is connected to the aforementioned second port, and whose cathode is connected to the gate terminal of the aforementioned first MOS transistor.

14. The level shifting circuit of Claim 13, comprising a second resistor connected in series with the aforementioned fourth diode between the aforementioned second port and the gate terminal of the aforementioned first MOS transistor.

15. The level shifting circuit of Claim 13, comprising a fourth constant current source circuit connected in series with the aforementioned fourth diode between the aforementioned second port and the gate terminal of the aforementioned first MOS transistor.

16. The level shifting circuit of one of Claims 1-15, wherein the aforementioned bias means is provided with a fifth diode whose anode is connected to the aforementioned power supply voltage terminal, and whose cathode is connected to the gate terminal of the aforementioned first MOS transistor.

17. The level shifting circuit of Claim 16, comprising

a third switch connected in series with the aforementioned fifth diode the aforementioned power supply voltage terminal and the gate terminal of the aforementioned first MOS transistor,

a fourth switch connected between the gate terminal of the aforementioned first MOS transistor and a reference potential logic level different from the aforementioned reference logic level, and

a switch control means that turns the aforementioned third switch on and the aforementioned fourth switch off and vice versa.

18. The level shifting circuit of Claim 17, comprising a voltage amplifier which increases the potential of the gate terminal of the aforementioned first MOS transistor to a level higher than the aforementioned power supply voltage in response to a control signal given by the aforementioned switch control means in order to turn the aforementioned third switch on and turn the aforementioned fourth switch off.

19. The level shifting circuit of Claim 18, wherein the aforementioned voltage amplifier circuit is provided with a delayed voltage output circuit that increases its output voltage from a logic level different from the aforementioned reference logic level to a logic level equal to the aforementioned reference logic level after a prescribed delay time has passed after the aforementioned control signal is input, as well as with a capacitor connected between the output terminal of the aforementioned delayed voltage output circuit and the gate terminal of the aforementioned first MOS transistor.

20. The level shifting circuit of one of Claims 1-17, comprising a third MOS transistor whose first terminal is connected to the aforementioned first port and whose second terminal is connected to the aforementioned second port,

a fourth MOS transistor of the same conductivity type as the aforementioned third MOS transistor whose first terminal is connected to the aforementioned power supply voltage terminal and whose second terminal and gate terminal are both connected to the gate terminal of the aforementioned third MOS transistor,

a sixth diode whose anode is connected to the aforementioned power supply voltage terminal and whose cathode is connected to the gate terminal of the aforementioned third MOS transistor,

a fifth switch connected in series with the aforementioned sixth diode between the aforementioned power supply voltage terminal and the gate terminal of the aforementioned third MOS transistor,

a sixth switch connected between the gate terminal of the aforementioned third MOS transistor and a reference potential having a logic level different from the aforementioned reference logic level,

a switch control means that turns the aforementioned fifth switch on and the aforementioned sixth switch off and vice versa, and

a voltage amplifier that increases the potential of the gate terminal of the aforementioned third MOS transistor to a level higher than the aforementioned power supply voltage in response to a control signal given by the aforementioned switch control means in order to turn the aforementioned fifth switch on and turn the aforementioned sixth switch off.

21. The level shifting circuit of Claim 20, wherein the aforementioned voltage amplifier is provided with a delayed voltage output circuit that increases its output voltage from a logic level different from the aforementioned reference logic level to a logic level equal to the aforementioned reference logic level after a prescribed amount of delay time has passed after the aforementioned control signal is input, as well as with a capacitor connected between the output terminal of the aforementioned delayed voltage output circuit and the gate terminal of the aforementioned third MOS transistor.

22. A level shifting circuit comprising a first MOS transistor connected between a first input/output terminal and a second input/output terminal,

a second MOS transistor connected between a first power supply voltage terminal and the gate terminal of the aforementioned first MOS transistor and whose gate terminal is connected to the gate terminal of the aforementioned first MOS transistor,

a first rectifying element connected between a first power supply voltage terminal and the gate terminal of the aforementioned first MOS transistor in order to source current from the first power supply voltage terminal to the gate terminal of the aforementioned first MOS transistor,

a second rectifying element connected between the aforementioned first input/output terminal and the gate terminal of the aforementioned first MOS transistor in order to source current from the aforementioned first input/output terminal to the gate terminal of the aforementioned first MOS transistor,

a third rectifying element connected between the aforementioned second input/output terminal and the gate terminal of the aforementioned first MOS transistor in order to source current from the aforementioned second input/output terminal to the gate terminal of the aforementioned first MOS transistor,

a third MOS transistor connected between the first power supply voltage terminal and the aforementioned first input/output terminal,

a fourth rectifying element connected between the aforementioned third MOS transistor and the aforementioned first input/output terminal in order to source current from the first power supply voltage terminal to the aforementioned first input/output terminal,

a fourth MOS transistor connected between the first power supply voltage terminal and the aforementioned second input/output terminal,

a fifth rectifying element connected between the aforementioned fourth MOS transistor and the aforementioned second input/output terminal in order to source current from the first power supply voltage terminal to the aforementioned second input/output terminal, and

a logic circuit whose first and second input terminals are connected to the aforementioned first and the second input/output terminals, respectively, in order to output a control signal to turn on the aforementioned fourth and fifth MOS transistors when the voltage level of the aforementioned first and/or the second input/output terminal corresponds to the aforementioned power supply voltage.

23. The level shifting circuit of Claim 22, wherein the aforementioned first and second MOS transistors are NMOS transistors,

the aforementioned third and fourth MOS transistors are PMOS transistors,

the aforementioned first rectifying element is a diode whose anode is connected to the first power supply voltage terminal and whose cathode is connected to the gate terminal of the aforementioned first MOS transistor,

the aforementioned second rectifying element is a diode whose anode is connected to the aforementioned first input/output terminal and whose cathode is connected to the gate terminal of the aforementioned first MOS transistor,

the aforementioned third rectifying element is a diode whose anode is connected to the aforementioned second input/output terminal and whose cathode is connected to the gate terminal of the aforementioned first MOS transistor,

the aforementioned fourth rectifying element is a diode whose anode is connected to the aforementioned third MOS transistor and whose cathode is connected to the aforementioned first input/output terminal, and

the aforementioned fifth rectifying element is a diode whose anode is connected to the aforementioned fourth MOS transistor and whose cathode is connected to the aforementioned second input/output terminal.

24. The level shifting circuit of Claim 22 or 23, comprising

a fifth MOS transistor connected between the aforementioned first rectifying element and the gate terminal of the aforementioned first MOS transistor in order to cut off the current path formed between the aforementioned first rectifying element and the gate terminal of the aforementioned first MOS transistor, the current path between the aforementioned second rectifying element and the gate terminal of the aforementioned first MOS transistor, and the current path between the aforementioned third rectifying element and the gate terminal of the aforementioned first MOS transistor,

a sixth MOS transistor connected between the gate terminal of the aforementioned first MOS transistor and the aforementioned second power supply voltage terminal, and

a control circuit that supplies a control signal in order to make the aforementioned fifth MOS transistor and the aforementioned sixth MOS transistor conductive in a complementary manner.